CENTRAL PROCESSOR UNIT (CPU) ASSEMBLY AND USER'S MANUAL

CPU BOARD

TABLE OF CONTENTS

INTRODUCTION

THE VECTOR GRAPHIC INC. CENTRAL PROCESSOR UNIT (CPU) PROVIDES ALL THE CENTRAL PROCESSING AND LOGIC FUNCTIONS FOR YOUR MICROCOMPUTER SYSTEM. THE HEART OF THIS BOARD IS THE 8080A LSI MICROPROCESSOR. COUPLED WITH THE SINGLE LSI CHIP ARE VARIOUS PERIPHERAL CIRCUITS TO PERFORM TIMING, CONTROL, BUS INTERFACE, AND POWER SUPPLY REGULATION TO OBTAIN A RELIABLE AND VERSATILE CPU.

ESPECAILLY USEFUL FEATURES OF THE VECTOR GRAPHIC CPU ARE THE 8 LEVEL VECTORED PRIORITY INTERRUPT CIRCUITS AND A REAL TIME CLOCK. PROVISION OF A REAL TIME CLOCK ALLOWS FOR SOPHISTICATED TIMING AND CONTROL FUNCTIONS ONLY FOUND IN ADVANCED INDUSTRIAL MINICOMPUTERS. A PROGRAMMABLE PRIORITY INTERRUPT STRUCTURE ALLOWS THE USER TO ASSIGN DIFFERENT LEVELS OF PRIORITIES OR IMPORTANCE OF THE INTERRUPT INPUTS TO THE MICROCOMPUTER. ASSIGNMENT OF PRIORITY LEVEL IS FULLY PROGRAMMABLE ALLOWING FOR ADAPTIVE OPERATION UNDER PROGRAM CONTROL.

ALL INTERFACE BETWEEN THE CPU BOARD AND THE STANDARD S-100 BUS ARE FULLY BUFFERED FOR ISOLATION AND RELIABLE OPERATION.

A STABLE CLOCK FOR THE 8080A IS PROVIDED BY A CRYSTAL CONTROLLED OSCILLATOR AND CLOCK DRIVER. THIS INSURES OPERATION OF THE 8080A WITHIN THE MANUFACTURERS SPECIFICATIONS FOR TROUBLE FREE OPERATION.

CAREFUL ATTENTION TO GOOD DESIGN PRACTICE PROVIDES USER WITH A CPU GUARANTEED TO OPERATE RELIABLY WITHOUT CONSTANT ADJUSTMENT AND MAINTENANCE.

ASSEMBLY INSTRUCTIONS

! CAUTION !

THE 8080A MICROPROCESSOR IS A MOS DEVICE AND THEREFORE SENSITIVE TO ELECTROSTATIC DISCHARGE. HANDLING OF THIS DEVICE SHOULD BE MINIMIZED AND IT SHOULD BE STORED IN THE PROTECTIVE HOLDER RECEIVED WITH THIS KIT.

COMMON SENSE PRECAUTION ON THE PART OF THE KIT BUILDER SHOULD BE EXERCISED TO ELIMINATE ANY EXCESSIVE ELECTROSTATIC CHARGES.

CPU BOARD KIT CONTENTS

QUANTITY	DESCRIPTION
	PRINTED CIRCUIT BOARD
1	8080A CENTRAL PROCESSOR A4
2	8212 8 BIT LATCH B6, C7
1	8214 PRIORITY INTERRUPT CONTROL UNIT C1
1	8224 CLOCK GENERATOR A5
9	8097/74367 HIGH SPEED HEX BUFFER INVERTERS A3, A8, B3, B4, B5, B7, C3, C4, C6
1	74LS02 QUADRUPLE 2-INPUT POSITIVE NOR GATE A2
2	74LS04 HEX INVERTER A6, C2
1	74LS74 DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP B1
1	74LS00 QUADRUPLE 2-INPUT POSITIVE NAND GATE B2
1	74LS30 8-INPUT POSITIVE NAND GATE C5
1	7805 REGULATOR
1	79L05 REGULATOR
1	78L12 REGULATOR
2	25 MFD 12V CAPACITORS
1	0.001 MFD. 1000V CERAMIC DISC CAPACITOR
11	0.1 MFD. 10V CERAMIC DISC CAPACITORS
2	150 PF 1000V CERAMIC DISC CAPACITORS
1	10 PF 600V CERAMIC DISC CAPACITORS
2	4.7 MFD. 50V ELECTROLYTIC CAPACITORS
2	27 OHM 1 WATT RESISTORS (BANDS OF RED, VIOLET, BLACK)
33	1K 1/4 WATT RESISTORS (BANDS OF BROWN, BLACK, RED)
2	47K 1/4 WATT RESISTORS (BANDS OF YELLOW, VIOLET, ORANGE)
9	4.7K 1/4 WATT RESISTORS (BANDS OF YELLOW, VIOLET, RED)
1	15K 1/4 WATT RESISTOR (BANDS OF BROWN, GREEN, ORANGE)
1	100 OHM 1/4 WATT RESISTOR (BANDS OF BROWN, BLACK, BROWN)
1	18 MHZ CRYSTAL
1	1N270 DIODE
1	LM358 OP-AMP
1	HEATSINK
1	40 PIN SOCKET
3	24 PIN SOCKETS
11	16 PIN SOCKETS
5	14 PIN SOCKETS
1	8 PIN SOCKET
1	#6-32 x 3/8 SCREW, NUT AND LOCKWASHER

TOOLS AND MATERIALS REQUIRED FOR ASSEMBLY

THE FOLLOWING MINIMUM SET OF TOOLS AND MATERIALS IS REQUIRED FOR THE ASSEMBLY OF VECTOR GRAPHIC INC. KITS:

DESCRIPTION	**COMMENT**
VOLT - OHMMETER	INEXPENSIVE
SCREWDRIVER - STRAIGHT SLOT	FOR #5 and #8 SCREWS
SCREWDRIVER - PHILLIPS HEAD*	FOR #8 SCREWS
CUTTERS - DIAGONAL	4", FLUSH CUTTING
PLIERS - NEEDLE NOSED	6"
PLIERS - REGULAR	MEDIUM
WIRE STRIPPER	FOR 8 AWG TO 20 AWG
SOLDERING IRON	30 WATTS MAXIMUM WITH CHISEL TIP
SOLDER	.030 GA. 60/40 TIN-LEAD ROSIN CORE
SPONGE	FOR CLEANING SOLDERING IRON
PEN KNIFE	OR 'X-ACTO KNIFE
CLEANING SOLVENT	TRICHLOROETHANE OR ISOPROPYL ALCOHOL. ***DO NOT USE ACETONE***
CARDBOARD	TO PROTECT TABLE TOP DURING SOLDERING
HEAT SINK GREASE	OR HIGH TEMPERATURE PLUMBERS GREASE
RULER*	TO MEASURE WIRE LENGTHS

*NOTE: REQUIRED FOR MAINFRAME CABINET ASSEMBLY ONLY

SOLDERING TECHNIQUE

THE SOLDER

USE A #20 GAUGE (.030") ROSIN CORE SOLDER WITH A RATIO OF AT LEAST 60% TIN AND 40% LEAD. "KESTER" AND "ERSIN" ARE TWO DEPENDABLE BRANDS OF SOLDER. ACID CORE SOLDERS OR ACID FLUX MUST NOT BE USED AS THEY WILL CORRODE THE PRINTED CIRCUIT BOARD.

THE SOLDERING IRON

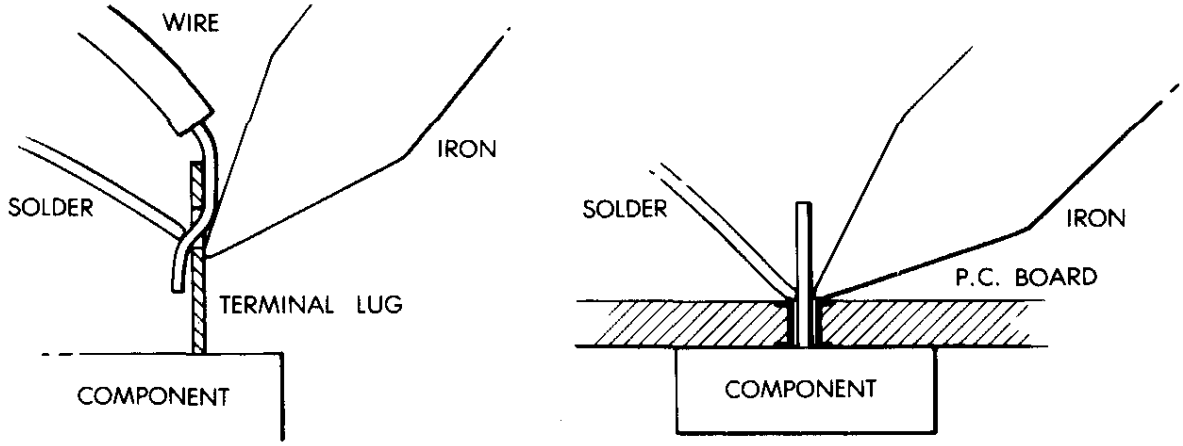
USE A SMALL, 30 WATT MAXIMUM IRON WITH A SMALL, CHISEL SHAPED TIP. TOO MUCH HEAT WILL DAMAGE BOTH COMPONENTS AND BOARDS. SOLDERING GUNS ARE TOO HOT AND SHOULD NOT BE USED.

HEAT THE IRON, WIPE ITS TIP QUICKLY ON THE DAMP SPONGE, AND APPLY A TINY AMOUNT OF SOLDER TO THE TIP - JUST ENOUGH TO MAKE IT SILVER IN COLOR BUT NOT SO MUCH THAT IT WILL DRIP OFF. THIS CLEANING PROCEDURE SHOULD BE REPEATED WHENEVER THE TIP OF THE SOLDERING IRON BEGINS TO TAKE ON A BROWNISH COLOR.

THE PROCEDURE

THE ENTIRE SOLDERING OPERATION SHOULD TAKE LITTLE MORE THAN TWO SECONDS PER JOINT. THE SEQUENCE IS AS FOLLOWS:

TOUCH THE TIP OF THE SOLDERING IRON TO THE JOINT, AS SHOWN BELOW, SO THAT BOTH CONDUCTORS TO BE JOINED ARE SIMULTANEOUSLY HEATED SUFFICIENTLY TO MELT THE SOLDER.



TOUCH THE SOLDER TO THE JOINT, AS SHOWN ABOVE, JUST LONG ENOUGH TO MELT ENOUGH SOLDER TO FORM A FILLET ON THE JOINT. TOO MUCH SOLDER MAY SHORT CIRCUIT THE BOTTOM OF THE BOARD OR FLOW THROUGH THE HOLES AND WICK INTO THE SOCKETS. THE MELTED SOLDER WILL APPEAR WET AND SHINY. IT WILL QUICKLY FLOW COMPLETELY AROUND THE WIRE AND OVER THE SURFACE TO WHICH THE WIRE IS ATTACHED.

REMOVE THE SOLDERING IRON AS SOON AS BOTH SURFACES HAVE BEEN COMPLETELY WETTED. REMEMBER, THE TOTAL TIME FROM APPLICATION TO REMOVAL OF THE SOLDERING IRON SHOULD BE ONLY TWO OR THREE SECONDS. REMOVAL OF THE SOLDERING IRON TOO SOON MAY RESULT IN A COLD SOLDER JOINT AND LEAVING THE SOLDERING IRON IN CONTACT TOO LONG MAY CAUSE HEAT DAMAGE TO EITHER THE COMPONENTS OR THE BOARD.

REMOVAL OF MULTI-PIN SOLDERED-IN PARTS

CAUTION

IF FOR ANY REASON, IT BECOMES NECESSARY TO REMOVE A SOLDERED-IN PART HAVING MORE THAN JUST TWO LEADS, DO NOT TRY TO REMOVE THE PART INTACT. IT CAN BE DONE BUT ONLY WITH RISK OF DAMAGING THE PRINTED CIRCUIT BOARD IN THE PROCESS.
HOLD THE PRINTED CIRCUIT BOARD IN A PADDED VISE TO AVOID DAMAGE.

REMOVAL OF SOLDERED-IN IC SOCKETS

CAREFULLY PRY UP THE PLASTIC BODY OF THE SOCKET USING A KNIFE OR SCREWDRIVER TO LEAVE THE PINS EXPOSED. GENTLY REMOVE THE PINS FROM THE TOP OF THE BOARD WITH NEEDLE NOSED PLIERS *WHILE TOUCHING THE JOINT* ON THE OTHER SIDE OF THE BOARD WITH THE TIP OF THE IRON. DO NOT USE FORCE. THE PIN WILL COME OUT QUITE EASILY ONCE THE SOLDER MELTS.
CLEAR THE HOLES OF ANY EXCESS SOLDER USING A SOLDER SUCKER OR WICK.

REMOVAL OF SOLDERED-IN INTEGRATED CIRCUIT CHIPS

CUT EACH PIN WITH A PAIR OF DIAGONAL CUTTERS AT A POINT BETWEEN THE CHIP AND THE PRINTED CIRCUIT BOARD WHICH IS AS CLOSE TO THE CHIP AS POSSIBLE SO THAT THERE IS ENOUGH OF THE PIN SHOWING ABOVE THE BOARD TO BE GRASPED BY NEEDLE NOSED PLIERS WHILE REMOVING AS DESCRIBED ABOVE.

PREPARATION FOR ASSEMBLY

WORKING AREA AND TOOLS

A WELL LIGHTED, CLEAN TABLE OR WORK BENCH AND THE PROPER TOOLS AND MATERIALS ARE MOST IMPORTANT FOR PRODUCING TROUBLE FREE ASSEMBLIES. THE WORK SURFACE SHOULD BE CLEAN AND FREE OF ALL ITEMS EXCEPT FOR THE TOOLS AND KIT COMPONENTS BEING USED. A CLEAN PIECE OF CARDBOARD OR HAND TOWEL IS SUGGESTED TO PROTECT THE TABLE TOP WHEN SOLDERING.

CHECK KIT CONTENTS

VERIFY THE CONTENTS OF YOUR KIT AGAINST THE KIT CONTENTS LIST IN THE FRONT OF THIS MANUAL. CHECK EACH PART VISUALLY FOR DAMAGE IN SHIPPING. IF THERE ARE ANY MISSING OR DAMAGED ITEMS, PLEASE NOTIFY THE DEALER FROM WHOM YOU BOUGHT YOUR KIT IMMEDIATELY. THERE MAY BE SLIGHT VARIATIONS FROM THE PARTS SPECIFIED, BUT THE COMPONENTS SHOULD BE FUNCTIONALLY EQUIVALENT.

PARTS LAYOUT AND ASSEMBLY SEQUENCE

THE FRONT OF THE BOARD IS THE SIDE ON WHICH THE PARTS LAYOUT HAS BEEN SILK SCREENED. ALL PARTS WILL BE ON THE FRONT OF THE PRINTED CIRCUIT BOARD. THEIR LEADS OR PINS WILL PASS THROUGH THE BOARD AND BE SOLDERED ON THE REAR.

PLACE THE BOARD WITH ITS FRONT SIDE UP AND THE GOLD EDGE CONTACTS NEAREST YOU. IN THAT POSITION, WE WILL REFER TO THE UPPER PORTION OF THE BOARD AS BEING FURTHEST AWAY FROM YOU.

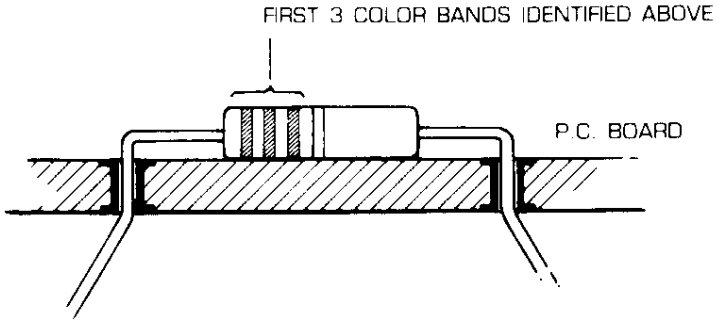
SHOULD YOU USE SOCKETS?

WE RECOMMEND THE USE OF SOCKETS FOR TWO REASONS. ONE IS THAT SOLDERED-IN CHIPS CANNOT BE RETURNED FOR REPLACEMENT. ANOTHER IS THAT, SHOULD YOU HAVE TO REPLACE A CHIP, IT IS POSSIBLE TO DO CONSIDERABLE DAMAGE TO THE P. C. BOARD, UNLESS YOU ARE EXPERIENCED AT IC REMOVAL AND HAVE THE PROPER TOOLS.

CPU BOARD ASSEMBLY SEQUENCE

INSERTION OF RESISTORS

ORIENTATION IS OF NO CONCERN WITH RESISTORS, BUT BE SURE THAT THE STRIPED COLOR CODE WHICH IDENTIFIES THE RESISTANCE VALUE IS AS SHOWN BELOW FOR THE PARTICULAR LOCATION.



33 1K 1/4 WATT RESISTORS (BANDS OF BROWN, BLACK, RED)
9 4.7K 1/4 WATT RESISTORS (BANDS OF YELLOW, VIOLET, RED)
2 47K 1/4 WATT RESISTORS (BANDS OF YELLOW, VIOLET, ORANGE)
1 15K 1/4 WATT RESISTOR (BANDS OF BROWN, GREEN, ORANGE)
1 100 OHM 1/4 WATT RESISTOR (BANDS OF BROWN, BLACK, BROWN)
2 27 OHM, 1 WATT RESISTORS (BANDS OF RED, VIOLET, BLACK)

DIODE

INSTALL THE 1N270 DIODE AS INDICATED ON THE ASSEMBLY DRAWING AND SOLDER. OBSERVE CORRECT POLARITY!!

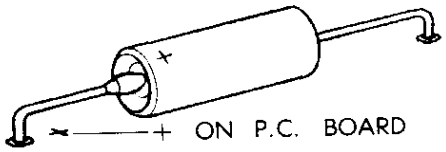
CRYSTAL

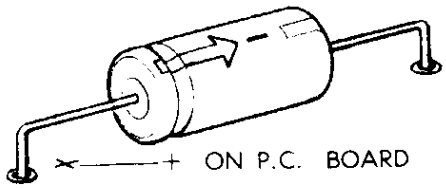
MEASURE AND BEND THE LEADS OF THE CRYSTAL. INSTALL THE CRYSTAL AS SHOWN ON THE ASSEMBLY DRAWING AND SOLDER. TIGHTLY LOOP A PIECE OF BARE HOOK UP WIRE OVER THE CRYSTAL AND INSTALL IN 2 HOLES ON EACH SIDE OF THE CRYSTAL. SOLDER THE WIRE IN PLACE.

AXIAL ELECTROLYTIC CAPACITORS

AGAIN REFERING TO THE COMPONENT PLACEMENT DIAGRAM, INSERT THE AXIAL ELECTROLYTIC CAPACITORS AND SOLDER IN PLACE IN THE SAME MANNER AS DESCRIBED FOR RESISTORS.

2 25 MFD 12V CAPACITORS
2 4.7 MFD 50V CAPACITORS





SOCKETS

PLACE THE PRINTED CIRCUIT BOARD (PCB) WITH THE VECTOR GRAPHIC INC. FACING DOWN, AND THE COMPONENT SIDE UP ON TOP OF THE TERRY CLOTH TOWEL. INSTALL THE SOCKETS WITH THE PIN 1 INDEX (TRIANGLE FILL IN) ON THE PCB IN THE FOLLOWING SEQUENCE. *DO NOT SOLDER!*

1 40 PIN SOCKET
3 24 PIN SOCKETS
11 16 PIN SOCKETS
5 14 PIN SOCKETS
1 8 PIN SOCKET

INSURE THAT NO 14 PIN SOCKETS ARE MISTAKENLY INSTALLED IN THE 16 PIN POSITIONS.

SOLDERING SOCKETS

ON EACH SOCKET, SOLDER TWO CORNER PINS THAT ARE DIAGONALLY OPPOSITE EACH OTHER. TOUCH THE PIN AND PAD WITH THE IRON TIP ALLOWING ENOUGH SOLDER TO FLOW TO FORM A RLET BETWEEN PIN AND PAD. AFTER DOING THIS TO ALL SOCKETS, RETURN TO THE FIRST AND SOLDER ALL PINS. USE A MINIMUM OF SOLDER TO AVOID SOLDER BRIDGES (SHORTS). AFTER ALL THE SOCKETS ARE CORRECTLY INSTALLED HOLD THE BOARD UP AND SIGHT ALONG THE SOCKETS TO BE SURE THAT THE PINS ARE PROPERLY SEATED. PLACE THE STIFF CARDBOARD OR MAGAZINE ON TOP OF THE SOCKETS TO HOLD THEM IN PLACE AND TURN THE BOARD OVER AND PLACE IT ON THE TOWEL. NOW PROCEED TO SOLDER ALL PINS ON THE SOCKETS.

INSERTION OF DISC CAPACITORS

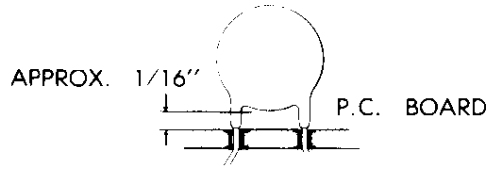
DISC CAPACITORS DO NOT REQUIRE SPECIAL ORIENTATION. HOWEVER, THEY OFTEN HAVE THEIR COATING EXTENDING DOWN FROM THEIR BODY ALONG THEIR LEADS. IF TOO FAR ALONG THE LEAD, IT MAY BE CRACKED OFF BY SQUEEZING IT WITH PLIERS. IN ANY EVENT, BE SURE THAT THIS INSULATIVE COATING DOES NOT EXTEND INTO THE PRINTED CIRCUIT BOARD HOLE.

INSERT THE LEADS OF THE 15 DISC CAPACITORS THROUGH THE PROPER HOLES AS INDICATED ON THE PARTS LAYOUT. BEND THE LEADS SLIGHTLY OUTWARD TO HOLD THE CAPACITOR IN POSITION WHILE SOLDERING. THE DISC CAPACITORS *SHOULD BE SPACED UNIFORMLY ABOVE THE PRINTED CIRCUIT BOARD ABOUT 1/16" SO AS TO GIVE A NEAT APPEARANCE* OF THE FINISHED BOARD. SOLDER IN PLACE WHILE HOLDING IN THIS POSITION.

CERAMIC DISC

REFERRING TO THE COMPONENT PLACEMENT DIAGRAM, BEND THE LEADS AND INSTALL THE DISC CAPACITORS IN THE FOLLOWING SEQUENCE AND SOLDER

11	0.1 MFD 10V CAPACITORS
2	150 PF 1000V CAPACITORS
1	10 PF 600V CAPACITOR
1	0.001 1000V MFD CAPACITOR

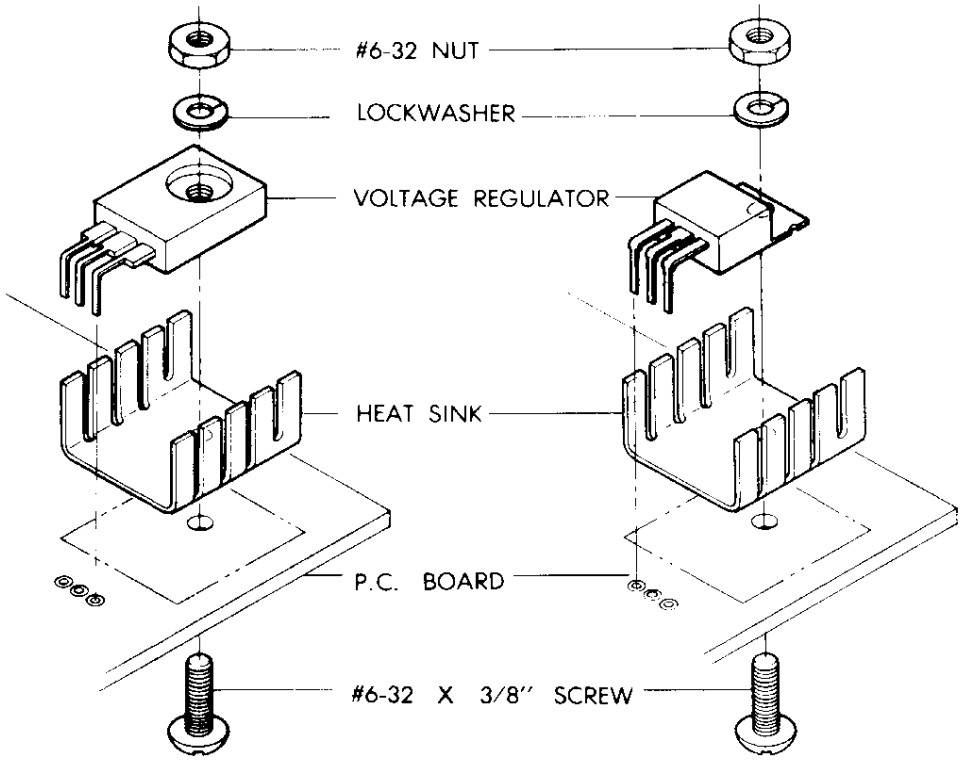


INSPECT FOR PROPER LOCATION AND FOR PROPER SOLDER JOINTS, AND THEN CLIP OFF EXCESS LEAD LENGTH WITH DIAGONAL CUTTER.

REGULATORS AND HEATSINK

PLACE THE +5V REGULATOR, 7805, ON THE BOARD SO THE MOUNTING HOLE IS IN LINE WITH THE HOLE IN THE BOARD. MEASURE THE LEADS FOR PROPER BENDING LOCATIONS AND BEND THEM AT RIGHT ANGLES. LEADS USE TWO LONG NOSE PLIERS ON EACH SIDE OF THE REGULATOR. DAMAGE TO THE REGULATOR MAY OCCUR IF BENDING STRESSES ARE APPLIED TO THE REGULATOR BODY. APPLY A SMALL AMOUNT OF HEAT SINK COMPOUND TO THE SIDE OF THE REGULATORS TO CONTACT THE HEAT SINKS. INSERT THE SCREW THROUGH THE BOARD FROM THE BACK, PLACE THE ALUMINUM HEAT SINK OVER THE SCREW. DROP THE REGULATOR IN PLACE ON TOP OF THE HEAT SINK AND FASTEN WITH WASHERS AND NUTS. SOLDER THE REGULATOR LEADS TO PADS ON THE BACK OF THE BOARD.

NEXT INSTALL THE +12V AND -5V REGULATORS AS INDICATED ON THE ASSEMBLY DRAWING. OBSERVE CORRECT ORIENTATION OF THE DEVICES.



PRELIMINARY TESTS

RRST INSTALL ALL OF THE INTEGRATED CIRCUITS WITH 14 OR 16 PINS. APPLY POWER TO THE BOARD BY PLUGGING IT INTO YOUR COMPUTER OR BY CONNECTING IT TO A SUITABLE POWER SUPPLY AND MEASURE THE REGULATED OUTPUT OF EACH REGULATOR. IF LESS THAN +4.75, -4.75, VOLTS IS MEASURED, CHECK FOR A SHORT CIRCUIT. *CAUTION! SHORTED REGULATORS SOMETIMES EXPLODE - - STAY CLEAR OF THE REGULATOR SIDE OF THE BOARD* WHILE TESTING IT. IF MORE THAN +5.25, -5.25, OR +12.6 VOLTS IS MEASURED, THE REGULATOR MAY BE BAD.

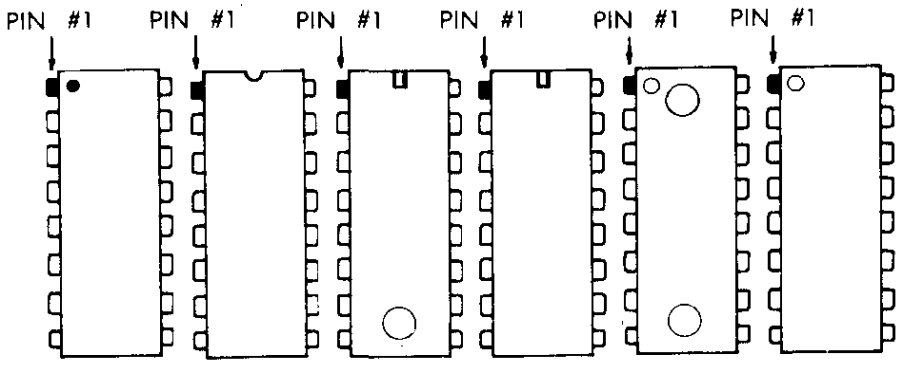
DO NOT CONTINUE WITHOUT MAKING THE FOLLOWING TEST. FAILURE TO DO SO COULD RUIN YOUR WHOLE DAY!

NEXT CHECK PIN 20 OF THE 40 PIN SOCKET FOR +5V, PIN 11 FOR -5V AND PIN 28 FOR +12V. FAILURE TO READ THESE VOLTAGES INDICATES MOST PROBABLY A SOLDER SHORT OR BROKEN RUN ON THE PCB.

ORIENTATION OF INTEGRATED CIRCUIT CHIPS

CARE MUST BE TAKEN TO INSURE THAT EACH INTEGRATED CIRCUIT CHIP IS SO ORIENTED, PRIOR TO INSERTION IN ITS SOCKET, THAT PIN #1 IS AT THE LOCATION SO DESIGNATED ON THE PRINTED CIRCUIT BOARD OR IN THE INDIVIDUAL ASSEMBLY INSTRUCTIONS FOR THE KIT.

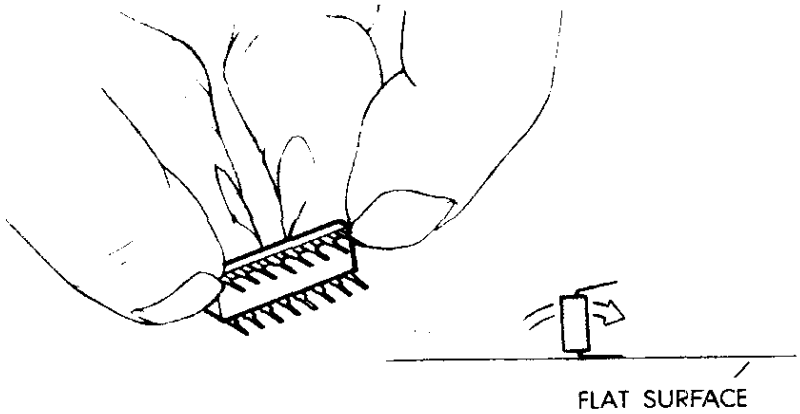
PIN #1 IS, UNFORTUNATELY, DESIGNATED IN A VARIETY OF WAYS DEPENDING UPON THE INTEGRATED CIRCUIT MANUFACTURER. SEVERAL METHODS ARE INDICATED IN THE DRAWING BELOW. WITH THE LEADS OF THE CHIP POINTING AWAY FROM THE VIEWER, PIN #1 IS IN THE POSITION INDICATED WITH RESPECT TO THE VARIOUS END NOTCHES OR TINY CIRCULAR MARKINGS OR DEPRESSIONS IN ONE CORNER.



INSERTION OF INTEGRATED CIRCUIT CHIPS

BE SURE ALL LEADS ARE STRAIGHT AND PARALLEL. IF NOT, GENTLY STRAIGHTEN AND ALIGN THE BENT PINS WITH NEEDLE NOSED PLIERS.

INTEGRATED CIRCUIT CHIPS USUALLY COME FROM THE MANUFACTURER WITH THEIR ROWS OF LEADS SPREAD WIDER THAN THE SOCKET. TO BEND THE PINS IN A UNIFORM MANNER, PLACE THE CHIP ON ITS SIDE ON A FLAT SURFACE SO THAT ONE ROW OF PINS IS FLAT AGAINST THE SURFACE AS SHOWN ON THE FOLLOWING PAGE.



HOLDING EACH SIDE OF THE CHIP FIRMLY AGAINST THE FLAT SURFACE WITH BOTH HANDS, ROTATE IT A SHORT DISTANCE UNTIL THE PINS ARE BENT PERPENDICULAR TO THE BODY.

INSTALLING THE INTEGRATED CIRCUITS:

PUT THE REST OF THE ICs INTO THE SOCKETS. BE SURE THE LEADS ARE NOT BENT AND THAT THE PIN 1 INDEX IS TOWARD THE LEFT OR TOWARD THE TOP OF THE BOARD. IT IS VERY EASY TO FOLD PINS UNDER THE CHIPS WHILE INSTALLING THEM.

CLEAN THE BOARD WITH A FLUX REMOVING SOLVENT, THE FLUX HAS NO ELECTRICAL EFFECT, AND MAY BE LEFT ON THE BOARD IF DESIRED.

FUNCTIONAL DESCRIPTION

THE VECTOR GRAPHIC CPU BOARD IS DESIGNED AROUND THE INTEL 8080A MICROPROCESSOR CHIP. THIS BOARD IS S-100 BUS COMPATIBLE WITH ALL "ALTAIR"™ AND IMSAI PRODUCTS, PROVIDING INTERCHANGEABILITY BETWEEN THE VARIOUS SYSTEMS.

SIMPLICITY OF DESIGN HAS BEEN STRESSED TO ENHANCE RELIABILITY OF OPERATION BY THE USE OF LSI AND MSI INTEGRATED CIRCUITS. THIS GOAL HAS BEEN ACHIEVED WHILE NOT SACRIFICING ANY LOSS IN PERFORMANCE.

INPUT POWER TO THE BOARD IS ±16V AND +8V. TO ACHIEVE THE REQUIRED LEVELS OF +12V AND ±5V, THREE VOLTAGE REGULATORS ARE USED. THEY ARE THE:

7805 FOR THE +5V (ON THE HEAT SINK)
79L05 FOR -5V
78L12 FOR +12V

AMPLE BYPASS AND FILTERING IS PROVIDED BY ELECTROLYTIC AND CERAMIC CAPACITORS DISTRIBUTED ON THE BOARD.

THE CENTRAL TIMING FUNCTION IS PROVIDED BY AN 8224 CLOCK GENERATOR I.C., WITH AN 18MHZ CRYSTAL USED AS THE PRIMARY FREQUENCY CONTROL ELEMENT FOR THE OSCILLATOR. THE OUTPUTS FROM THIS CHIP ARE Ø1 AND Ø2 FOR THE 8080A PLUS A Ø2 SUITABLE FOR DRIVING TTL CIRCUITS. BUFFERED Ø1 AND Ø2 CLOCKS ARE AVAILABLE ON THE S-100 BUS ON PINS 25(Ø1) AND 24(Ø2).

PROCESSOR TIMING IS DIVIDED INTO TWO BASIC CYCLES. THEY ARE THE MACHINE CYCLE AND INSTRUCTION CYCLE. AN INSTRUCTION CYCLE IS DEFINED AS THE TIME REQUIRED TO FETCH AND EXECUTE AN INSTRUCTION. DURING THE FETCH CYCLE A SELECTED INSTRUCTION IS READ FROM MEMORY AND DEPOSITED IN THE CPU. DURING THE EXECUTION PHASE THE INSTRUCTION IS DECODED AND TRANSLATED INTO SPECIFIC PROCESSING ACTIVITIES. EVERY INSTRUCTION CYCLE CONSISTS OF FROM ONE TO FIVE MACHINE CYCLES. A MACHINE CYCLE IS NEEDED EACH TIME THE PROCESSOR ACCESSES MEMORY OR AN I/O PORT. EACH MACHINE CYCLE CONSISTS OF FROM THREE TO FIVE STATES. A STATE IS DEFINED AS THE INTERVAL BETWEEN TWO Ø1 CLOCK PULSES.

THE 8224 PROVIDES THE RESET AND READY INPUTS TO THE 8080A. THESE SIGNALS ARE SYNCHRONIZED TO THE Ø2 CLOCK PULSE AND ARE INITIATED FROM S-100 BUS INPUTS. A RESET MAY BE GENERATED BY THE PRESET (PIN 75) INPUT FROM THE S-100 BUS OR BY AN RC TIME CONSTANT ON THE BOARD WHEN THE SYSTEM IS INITIALLY TURNED ON. THE RESET SIGNAL ALSO GENERATES THE POWER ON CLEAR POC (PIN 99) OUTPUT ON THE S-100 BUS.

THE READY OUTPUT FROM THE 8224 INDICATES TO THE 8080A THAT VALID DATA IS AVAILABLE ON THE INPUT DATA LINES. THIS SIGNAL IS GENERATED BY THE PRDY (PIN 72) OR XRDY (PIN 3) INPUTS FROM THE S-100 BUS. FOR EXAMPLE, THE VECTOR GRAPHIC PROM/RAM BOARD GENERATES THE PRDY SIGNAL WHEN DATA IS AVAILABLE FROM THAT BOARD FOR USE BY THE CPU.

DATA I/O LINES ON THE 8080A ARE D0 TO D7. THESE LINES ALLOW FUNCTIONAL DATA COMMUNICATION BETWEEN THE 8080A AND THE REST OF THE COMPUTER SYSTEM. INTERFACE BETWEEN THE 8080A DATA LINES AND THE S-100 BUS IS THROUGH 8097 TRI STATE BUS DRIVERS. THESE CIRCUITS ALLOW THE 8080A TO OUTPUT DATA TO THE DO BUS OR INPUT DATA FROM THE DI BUS AT THE CORRECT TIMES. STATUS SIGNALS DESCRIBING THE CURRENT MACHINE CYCLE ARE PROVIDED ON THE 8080A DATA LINES DURING THE FIRST PART OF EACH MACHINE CYCLE. THIS INFORMATION IS STORED IN AN 8212 8 BIT STATUS LATCH WHICH IS GATED ON TO THE S-100 BUS BY 8097 DRIVERS AT THE CORRECT TIME. THE FUNCTION OF EACH STATUS SIGNAL ON THE S-100 BUS IS DEFINED BELOW.

1.	+8V	UNREGULATED INPUT TO +5V REGULATORS
2.	+16V	UNREGULATED INPUT TO +12V REGULATORS
3.	XRDY	ANDED WITH PRDY AND GOES TO 8080 RDY
4.	VIØ	VECTORED INTERRUPT REQUEST Ø
5.	VI1	VECTORED INTERRUPT REQUEST 1
6.	VI2	VECTORED INTERRUPT REQUEST 2
7.	VI3	VECTORED INTERRUPT REQUEST 3
8.	VI4	VECTORED INTERRUPT REQUEST 4
9.	VI5	VECTORED INTERRUPT REQUEST 5
10.	VI6	VECTORED INTERRUPT REQUEST 6
11.	VI7	VECTORED INTERRUPT REQUEST 7
12.	XRDY2	
13.		
14.		
15.		
16.		
17.		
18.	$\overline{\text{STA DSB}}$	STATUS BUFFER DISABLE
19.	$\overline{\text{C/C DSB}}$	COMMAND/CONTROL BUFFER DISABLE
20.	UNPROT	INPUT TO MEMORY PROTECT CIRCUITRY ON MEMORY BD.
21.	SS	INDICATES MACHINE IS IN SINGLE STEP MODE
22.	$\overline{\text{ADD DSB}}$	ADDRESS BUFFER DISABLE
23.	$\overline{\text{DO DSB}}$	DATA OUT (FROM CPU) BUFFER DISABLE
24.	Ø1	PHASE TWO CLOCK TTL LEVELS
25.	Ø2	PHASE ONE CLOCK TTL LEVELS

26.	PHLDA	HOLD ACKNOWLEDGE, BUFFERED 8080 OUTPUT
27.	PWAIT	WAIT ACKNOWLEDGE, BUFFERED 8080 OUTPUT
28.	PINTE	INTERRUPT ENABLE, BUFFERED 8080 OUTPUT
29.	A5	BUFFERED ADDRESS LINE 5 [32]
30.	A4	BUFFERED ADDRESS LINE 4 [16]
31.	A3	BUFFERED ADDRESS LINE 3 [8]
32.	A15	BUFFERED ADDRESS LINE 15 [32768]
33.	A12	BUFFERED ADDRESS LINE 12 [4096]
34.	A9	BUFFERED ADDRESS LINE 1 [2]
35.	DO1	BUFFERED DATA OUT LINE 1
36.	DOØ	BUFFERED DATA OUT LINE Ø
37.	A1Ø	BUFFERED ADDRESS LINE 1Ø [1024]
38.	DO4	BUFFERED DATA OUT LINE 4
39.	DO5	BUFFERED DATA OUT LINE 5
40.	DO6	BUFFERED DATA OUT LINE 6
41.	D12	DATA INPUT LINE 2
42.	D13	DATA INPUT LINE 3
43.	D17	DATA INPUT LINE 7
44.	SMI	LATCHED 8080 M1 STATUS
45.	SOUT	LATCHED 8080 OUT STATUS
46.	SINP	LATCHED 8080 INP STATUS
47.	SMEMR	LATCHED 8080 MEMR STATUS
48.	SHLTA	LATCHED 8080 HLTA STATUS
49.	CLOCK	2 MHZ CLOCK, CRYSTAL CONTROLLED

VECTOR GRAPHIC INC.

50. GND LOGIC AND POWER GROUND RETURN

51. +8V UNREGULATED INPUT TO +5V REGULATORS

52. -16V UNREGULATED INPUT TO NEGATIVE REGULATORS

53. $\overline{\text{SSW DSB}}$ SENSE SWITCH DISABLE

54. $\overline{\text{EXT CLR}}$ CLEAR SIGNAL FOR I/O DEVICES

55. CHASSIS GROUND

56. $\overline{\text{STSTB}}$ STROBE SIGNAL (BY 8224 CLOCK CHIP 8800B D/C BOARD)

57. DIGI ENABLE SIGNAL FOR CPU DI DRIVERS 8800B

58. FRDY 8800B FRONT PANEL READY SIGNAL

59.

60.

61.

62.

63.

64.

65.

66.

67. $\overline{\text{PHANTOM}}$

68. MWRT WRITE ENABLE SIGNAL FOR MEMORY

69. $\overline{\text{PS}}$ INDICATES IF ADDRESSED MEMORY IS PROTECTED

70. PROT INPUT TO MEMORY PROTECT CIRCUITRY ON MEMORY BD.

71. RUN INDICATES MACHINE IS IN RUN MODE

72. PRDY ANDED WITH XRDY AND GOES TO 8080 RDY

73. $\overline{\text{PINT}}$ INPUT TO 8080 INTERRUPT REQUEST

74. $\overline{\text{PHOLD}}$ INPUT TO 8080 HOLD REQUEST

75. $\overline{\text{PRESET}}$ CLEAR SIGNAL FOR CPU

76. PSYNC BUFFERED 8080 SYNC SIGNAL

77. $\overline{\text{PWR}}$ BUFFERED 8080 WRITE ENABLE SIGNAL

78. PDBIN BUFFERED 8080 BDIN SIGNAL

79. AØ BUFFERED ADDRESS LINE Ø (1)

80. A1 BUFFERED ADDRESS LINE 1 (2)

81. A2 BUFFERED ADDRESS LINE 2 (4)

82. A6 BUFFERED ADDRESS LINE 6 (64)

83. A7 BUFFERED ADDRESS LINE 7 (128)

84. A8 BUFFERED ADDRESS LINE 8 (256)

85. A13 BUFFERED ADDRESS LINE 13 (8192)

86. A14 BUFFERED ADDRESS LINE 14 (16384)

87. A11 BUFFERED ADDRESS LINE 11 (2048)

88. DO2 BUFFERED DATA OUT LINE 2

89. DO3 BUFFERED DATA OUT LINE 3

90. DO7 BUFFERED DATA OUT LINE 7

91. DI4 DATA INPUT LINE 4

92. DI5 DATA INPUT LINE 5

93. DI6 DATA INPUT LINE 6

94. DI1 DATA INPUT LINE 1

95. DIØ DATA INPUT LINE Ø

96. SINTA LATCHED 8080 INTA STATUS

97. $\overline{\text{SWO}}$ LATCHED 8080 WO STATUS

98. SSTACK LATCHED 8080 STACK STATUS

99. $\overline{\text{POC}}$ LO DURING POWER UP, RESET

100. GND LOGIC AND POWER GROUND RETURN

VECTOR GRAPHIC INC.

STATUS SIGNAL DEFINITIONS

SIGNAL	DEFINITION
SINTA [PIN 96]	ACKNOWLEDGE SIGNAL FOR AN INTERRUPT REQUEST
SWO [PIN 97]	INDICATES THAT THE CURRENT MACHINE CYCLE IS A MEMORY WRITE OR OUTPUT OPERATION.
SSTACK [PIN 98]	INDICATES THAT THE ADDRESS BUS HOLDS THE PUSHDOWN STACK ADDRESS FROM THE STACK POINTER
SHLTA [PIN 48]	ACKNOWLEDGE SIGNAL FOR THE HALT INSTRUCTION
SOUT [PIN 45]	INDICATES THAT THE ADDRESS BUS CONTAINS THE ADDRESS OF AN OUTPUT DEVICE
SMI [PIN 44]	INDICATES THAT THE 8080A IS IN THE FETCH CYCLE FOR THE FIRST BYTE OF AN INSTRUCTION
SINP [PIN 46]	INDICATES THAT THE ADDRESS BUS CONTAINS THE ADDRESS OF AN INPUT DEVICE
SMEMR [PIN 47]	INDICATES THAT THE BUS WILL BE USED FOR A MEMORY READ OPERATION

A SOCKET CONNECTOR TO THE 8080A DATA LINES IS ALSO PROVIDED IN THE EVENT IT IS NEEDED TO INTERFACE A CONTROL PANEL TO THE CPU BOARD.

THERE ARE SIXTEEN ADDRESS LINES ON THE 8080A. THIS ALLOWS THE CPU TO ACCESS UP TO 65,536(64K WHERE K = 1024) MEMORY LOCATIONS. THESE ADDRESS LINES ARE CONNECTED TO THE S-100 BUS THROUGH 8097 DRIVERS AND GATED AT APPROPRIATE TIMES.

A POWERFUL PRIORITY VECTORED INTERRUPT STRUCTURE IS PROVIDED ON THE CPU BOARD. THIS IS ACCOMPLISHED USING AN 8214 PRIORITY INTERRUPT CONTROL I.C. AND AN 8212 LATCH TO GENERATE THE RST INSTRUCTION. THESE CIRCUITS ALLOW THE VECTOR GRAPHIC MICROCOMPUTER TO OPERATE AS A REAL TIME INTERRUPT DRIVEN COMPUTER SYSTEM. FOR A DETAILED DESCRIPTION OF THE THEORY OF INTERRUPTS REFER TO THE INTEL 8080A MICROCOMPUTER SYSTEMS MANUAL.

THERE ARE EIGHT INTERRUPT INPUTS TO THE COMPUTER, VI0 TO VI7, WHICH ARE CONNECTED TO THE 8214 I.C. WHEN AN INTERRUPT IS SENSED BY THE 8214, A SYNCHRONIZED INTERRUPT SIGNAL IS SENT TO THE 8080A. THE NUMBER OF THE INTERRUPT IS ENCODED AND SENT TO THE 8212 FOR USE IN GENERATING THE ADDRESS FOR THE INTERRUPT HANDLING SOFTWARE UNIQUE TO THAT INTERRUPT. THE PRIORITY FUNCTION IS PROVIDED WHEN MORE THAN ONE INTERRUPT IS RECEIVED BY THE 8214 BY COMPARING THE NUMBERS OF THE INTERRUPTS WITH A PRIORITY LEVEL STORED IN THE DEVICE. THIS PRIORITY LEVEL IS DETERMINED BY THE USER AND MAY BE CHANGED UNDER SOFTWARE CONTROL. THE INTERRUPT OF HIGHEST PRIORITY IS THE ONE WHICH IS PROCESSED.

OTHER INTERRUPT REQUESTS MAY BE GENERATED AND ENTERED INTO THE CPU BOARD BY THE PINT [PIN 73] INPUT FROM THE S-100 BUS. THE 8080A MAY BE REQUESTED TO ENTER THE HOLD STATE BY THE PHOLD [PIN74] INPUT FROM THE S-100 BUS. THE HOLD STATE ALLOWS AN EXTERNAL DEVICE TO GAIN CONTROL OF THE ADDRESS AND DATA LINES. WHEN THE PHOLD SIGNAL IS REMOVED THE 8080A RESUMES NORMAL PROCESSING.

ANOTHER POWERFUL FEATURE OF THE VECTOR GRAPHIC CPU BOARD IS THE PROVISION OF A REAL TIME CLOCK. THIS FEATURE ALLOWS THE USER TO GENERATE A REAL TIME CLOCK OR EXECUTE TIME SEQUENCED OPERATIONS. A STABLE OP-AMP DIFFERENTIATOR SENSES THE 120 HZ RIPPLE ON THE +8V LINE TO GENERATE PRECISE 8.33 MSEC TIME INTERVALS. JUMPER CONNECTIONS ARE PROVIDED FROM THE CLOCK TO THE VECTORED INTERRUPT INPUTS. UNDER SOFTWARE CONTROL THE USER CAN GENERATE 8.33MSEC INTERRUPTS TO THE 8080A FOR TIMING OPERATIONS.

THERE ARE NUMEROUS ACKNOWLEDGE AND CONTROL SIGNALS FROM THE 8080A AVAILABLE ON THE S-100 BUS. THESE SIGNALS ARE USEFUL FOR DETERMINING MACHINE STATUS AND CONTROLLING PERIPHERAL OPERATIONS. THEY ARE DERNED BELOW.

ACKNOWLEDGE AND CONTROL SIGNALS

SIGNAL	DEFINITION
PSYNC (PIN 76)	PROVIDES A SIGNAL TO INDICATE THE BEGINNING OF EACH MACHINE CYCLE
PWR (PIN 77)	USED FOR MEMORY WRITE OR I/O OPERATIONS. DATA IS STABLE WHEN PWR IS LOW
PDBIN (PIN 78)	INDICATES THAT THE 8080A DATA BUS IS IN THE INPUT MODE
PINTE (PIN 28)	INDICATES CONTENTS OF THE 8080A INTERRUPT ENABLE FLIP FLOP
PHLDA (PIN 26)	INDICATES THAT THE 8080A IS IN THE HOLD STATE
PWAIT (PIN 27)	INDICATES THAT THE 8080A IS IN THE WAIT STATE

THERE ARE A NUMBER OF SIGNALS WHICH WILL DISABLE VARIOUS PORTIONS OF THE S-100 BUS. WHEN THESE SIGNALS ARE ACTIVE THEY EFFECTIVELY DISCONNECT THAT PORTION OF THE CPU BOARD FROM THE S-100 BUS, THUS ALLOWING EXTERNAL DEVICES TO CONTROL THE S-100 BUS. THIS FEATURE IS USEFUL IN DMA APPLICATIONS AND MULTIPROCESSOR SYSTEMS. THEY ARE DEFINED BELOW.

S-100 BUS DISABLE SIGNALS

SIGNAL	FUNCTION
CC DSBL (PIN 19)	DISABLES THE ACKNOWLEDGE AND CONTROL SIGNALS
ADDR DSBL (PIN 22)	DISABLES THE ADDRESS LINES
DO DSBL (PIN 23)	DISABLES THE OUTPUT DATA LINES
SSW DSBL (PIN 53)	DISABLES THE INPUT DATA LINES
STAT DSBL (PIN 18)	DISABLES THE STATUS LINES

ALL S-100 BUS INTERFACES ARE PROVIDED WITH APPROPRIATE PULL UP RESISTORS FOR OPTIMUM RESPONSE OF SIGNALS ON THE BUS.

JUMPER INSTALLATION

IF IT IS DESIRED TO USE THE REAL TIME CLOCK FUNCTION ON THE CPU BOARD, A JUMPER MUST BE INSTALLED TO SELECT WHICH INTERRUPT THE CLOCK WILL ACTIVATE. ONLY ONE JUMPER SHOULD BE USED. THIS JUMPER WILL CONNECT THE REAL TIME CLOCK OUTPUT TO THE DESIRED INTERRUPT INPUT. FOR EXAMPLE IF ONE WISHES TO HAVE THE CLOCK ENTER ON INTERRUPT NUMBER 5 THEN A JUMPER SHOULD BE INSTALLED FROM THE CLOCK TO THE V15 INTERRUPT.

A PAD IS PROVIDED ON THE PRINTED CIRCUIT BOARD AT THE OUTPUT OF THE REAL TIME CLOCK. THIS POINT IS IDENTIFIED ON THE ASSEMBLY DRAWING AS RTC. SIMPLY SOLDER A WIRE FROM RTC TO THE DESIRED INTERRUPT VI0 TO VI7. PADS ARE PROVIDED FOR EACH INTERRUPT AND ARE LABELED VI0, VI1, VI2, VI3, VI4, VI5, VI6, AND VI7.

CLOCK DEMONSTRATION PROGRAM

A PROGRAM TO DEMONSTRATE THE USE OF INTERRUPTS AND THE REAL TIME CLOCK (RTC) IS LISTED ON THE FOLLOWING PAGES. IN ORDER TO RUN THE PROGRAM, THE RTC INTERRUPT MUST BE JUMPERED ON THE CPU BOARD TO VIO, WHICH CAUSES A "RST 7" TO BE EXECUTED ON INTERRUPT. THIS IS DONE BY SOLDERING A JUMPER BETWEEN THE TWO BOTTOM PADS IN THE COLUMN OF PADS IMMEDIATELY TO THE RIGHT OF C1. A VIDEO DISPLAY IS ASSUMED AT ADDRESS D000.

THE PROGRAM CAN BE LOADED INTO RAM ON THE PROM/RAM BOARD AT CC00 USING THE "P" COMMAND FROM THE MONITOR AND THEN SAVED ON TAPE. EXECUTE THE PROGRAM INITIALLY AT CCB4 (TEST), WHICH HAS A DELAY LOOP TO SIMULATE THE RTC. THIS DOES NOT USE THE INTERRUPTS, BUT WILL DISPLAY AN INCREMENTING TIME ON THE SCREEN TO MAKE SURE THE PROGRAM IS FUNCTIONING.

NOTE: IF YOU HAVE A 3P+S BOARD IN YOUR SYSTEM, CHECK TO MAKE SURE THAT UNUSED CIRCUITRY IS NOT PULLING SOME OF THE INTERRUPT LINES LOW. IT IS NECESSARY TO LEAVE SEVERAL OF THE IC'S OUT IF THEIR INPUTS ARE NOT CONNECTED.

IF THE PROGRAM APPEARS TO BE FUNCTIONING, EXECUTE AT CC00. THE FIRST INSTRUCTIONS WRITE THE "JMP COUNT" INSTRUCTIONS AT LOCATION 0038F IN MEMORY, INITIALIZE THE CURRENT STATUS REGISTER IN THE 8214 PRIORITY ENCODER BY OUTPUTTING 8 TO PORT FD, AND ENABLE THE INTERRUPT FLIP-FLOP IN THE MPU. THIS MUST BE DONE INITIALLY SINCE A POWER UP OR RESET ALSO RESETS THE INTERRUPT FLIP-FLOP, AND IT MUST BE REPEATED AFTER EACH INTERRUPT, WHICH AUTOMATICALLY RESETS THE 8214 AND DISABLES INTERRUPTS. AT THE END OF THIS ROUTINE, EXECUTION RETURNS TO THE MONITOR, OR ANY OTHER PROGRAM THAT INITIALLY CALLS "START".

AN INTERRUPT, WHICH OCCURS EVERY 1/120TH SECOND, CAUSES NORMAL PROGRAM EXECUTION TO BE SUSPENDED, AND THE "COUNT" ROUTINE TO BE EXECUTED. SINCE MANY PROGRAMS HAVE A LIMITED SPACE ALLOCATED FOR THE STACK, THE STACK POINTER IS SAVED AND THE STACK IS REINITIALIZED BELOW THE VIDEO DRIVER STORAGE LOCATIONS AND THEN ALL MPU REGISTERS ARE SAVED. NOTICE THE ORDER IN WHICH THIS IS DONE. THE PSW MUST BE SAVED ON THE OLD STACK BECAUSE DAD SP CHANGES THE CY FLAG.

A CALL TO "TICK" INCREMENTS THE TIME DIGITS STORED AT FACE IN BCD FORMAT AND PROPOGATES A CARRY AS EACH DIGIT OVERFLOWS. THE NUMBER LOADED IN THE "B" REGISTER WHEN "TOCK" IS CALLED DETERMINES THE MODULUS OF EACH REGISTER IN BCD, NOT BINARY. FOR EXAMPLE, THE FIRST CALL TO "TOCK" DIVIDES THE INTERRUPT FREQUENCY BY 12 TO PRODUCE A 10 HZ COUNT RATE. IF THE INCREMENTED REGISTER DOES NOT OVERFLOW, "TOCK" RETURNS TWO LEVELS. THE FIRST DIGIT REGISTER IS EXAMINED, AND IF IT IS ZERO, INDICATING THAT THE TIME HAS CHANGED AND THE DISPLAY MUST BE UPDATED, "DISP" IS CALLED, WHICH WRITES THE DIGITS ON THE UPPER RIGHT HAND CORNER OF THE SCREEN IN THE FOLLOWING FORMAT:

AM - 09:36:25.3

THE TIME IS IN A MODIFIED MILITARY FORMAT; I.E., HALF PAST MIDNIGHT OR NOON = 00:30:00.0

BEFORE RETURNING TO THE PROGRAM INTERRUPTED, THE MPU REGISTERS AND THE STACK POINTER ARE RESTORED, AND INTERRUPTS ARE ENABLED.

THE PROGRAM CAN BE USED WITH OTHER PROGRAMS THAT DO NOT USE THE RST 7 LOCATION OR DEPEND ON CRITICAL TIMING. INCLUDED IN THIS GROUP IS MITS BASIC. THE START ROUTINE WILL OVERWRITE BASIC WITH THE NECESSARY CODE, INCLUDING EI AT LOCATION 0000, WHICH PERMITS RETURNING TO BASIC WITH THE CLOCK RUNNING.

THE PROGRAM CAN BE USED WITHOUT CHANGES WITH THE FOLLOWING VIDEO BOARDS:

VECTOR GRAPHIC FLASH WRITER
VDM-1
POLYMORPHIC VTI
SOLID STATE MUSIC

OPTIONALLY, "PBIAS" CAN BE SET TO 0 FOR ALL OF THE ABOVE EXCEPT VTI IF REVERSE VIDEO IS NOT DESIRED.

THE TIME IS SET USING THE MONITOR "P" COMMAND BY MODIFYING MEMORY LOCATIONS CC16 THROUGH CC1B.

```
CC00                                0001 * CLOCK DEMONSTRATION PROGRAM
CC00                                0002 * R. S. HARP 9/4/77
CC00                                0004 PBIAS  EQU   80H
CC00                                0005 *
CC00                                0006 * THIS ROUTINE PUTS THE PROPER CODE AT RST 7
CC00 21 38 00                       0010 START  LXI   H,38H          RST 7
CC03 36 C3                          0020        MVI   M,0C3H
CC05 21 1C CC                       0030        LXI   H,COUNT
CC08 22 39 00                       0040        SHLD  39H
CC0B 3E FB                          0050        MVI   A,0FBH         ENABLE INTER.
CC0D 32 00 00                       0060        STA   0
CC10 3E 08                          0070        MVI   A,008H
CC12 D3 FD                          0080        OUT   0FDH           SET CUR STAT LATCH
CC14 FB                             0090        EI
CC15 C9                             0100        RET
CC16                                0110 FACE   DS    6              STORAGE FOR TIME
CC1C E5                             0140 COUNT  PUSH  H              MOVE THE STACK
CC1D F5                             0145        PUSH  PSW
CC1E 21 00 00                       0150        LXI   H,00
CC21 39                             0160        DAD   SP
CC22 31 00 CF                       0170        LXI   SP,0CF00H
CC25 E5                             0180        PUSH  H
CC26 C5                             0190        PUSH  B
CC27 D5                             0200        PUSH  D
CC28 21 16 CC                       0210        LXI   H,FACE
CC2B CD 87 CC                       0220        CALL  TICK
CC2E 21 16 CC                       0230        LXI   H,FACE
CC31 7E                             0240        MOV   A,M
CC32 B6                             0250        ORA   M
CC33 CC 42 CC                       0260        CZ    DISP
CC36 3E 08                          0270        MVI   A,008H
CC38 D3 FD                          0280        OUT   0FDH
CC3A D1                             0290        POP   D
CC3B C1                             0300        POP   B
CC3C E1                             0310        POP   H
CC3D F9                             0320        SPHL
CC3E F1                             0330        POP   PSW
CC3F E1                             0340        POP   H
CC40 FB                             0350        EI
CC41 C9                             0360        RET
CC42                                0365 * FORMAT THE DISPLAY
CC42 11 3F D0                       0370 DISP   LXI   D,0D03FH
CC45 23                             0380        INX   H
CC46 CD 70 CC                       0390        CALL  WRT2
CC49 23                             0400        INX   H
CC4A 36 AE                          0410        MVI   M,'.'+PBIAS
CC4C EB                             0420        XCHG
CC4D 1B                             0430        DCX   D
CC4E CD 70 CC                       0440        CALL  WRT2
CC51 36 BA                          0450        MVI   M,':'+PBIAS
CC53 EB                             0460        XCHG
CC54 1B                             0470        DCX   D
CC55 CD 70 CC                       0480        CALL  WRT2
CC58 36 BA                          0490        MVI   M,':'+PBIAS
```

```
CC5A EB                  0500          XCHG
CC5B 1B                  0510          DCX   D
CC5C CD 70 CC            0520          CALL  WRT2
CC5F EB                  0530          XCHG
CC60 46                  0540          MOV   B,M
CC61 EB                  0550          XCHG
CC62 36 AD               0560          MVI   M,'-'+PBIAS
CC64 2B                  0570          DCX   H
CC65 36 CD               0580          MVI   M,'M'+PBIAS
CC67 2B                  0590          DCX   H
CC68 AF                  0600          XRA   A
CC69 B8                  0610          CMP   B
CC6A 36 C1               0620          MVI   M,'A'+PBIAS
CC6C C8                  0630          RZ
CC6D 36 D0               0640          MVI   M,'P'+PBIAS
CC6F C9                  0650          RET
CC70                     0655 * WRITE THE DIGITS ON THE SCREEN
CC70 7E                  0660 WRT2     MOV   A,M
CC71 E6 0F               0670          ANI   00FH
CC73 F6 B0               0680          ORI   30H+PBIAS
CC75 EB                  0690          XCHG
CC76 77                  0700          MOV   M,A
CC77 EB                  0710          XCHG
CC78 1B                  0720          DCX   D
CC79 7E                  0730          MOV   A,M
CC7A 1F                  0740          RAR
CC7B 1F                  0750          RAR
CC7C 1F                  0760          RAR
CC7D 1F                  0770          RAR
CC7E E6 0F               0780          ANI   00FH
CC80 F6 B0               0790          ORI   30H+PBIAS
CC82 EB                  0800          XCHG
CC83 77                  0810          MOV   M,A
CC84 2B                  0820          DCX   H
CC85 13                  0830          INX   D
CC86 C9                  0840          RET
CC87                     0845 * INCREMENT THE TIME
CC87 06 12               0850 TICK     MVI   B,012H
CC89 CD A6 CC            0860          CALL  TOCK
CC8C 06 10               0870          MVI   B,010H
CC8E CD A6 CC            0880          CALL  TOCK
CC91 06 60               0890          MVI   B,060H
CC93 CD A6 CC            0900          CALL  TOCK
CC96 06 60               0910          MVI   B,060H
CC98 CD A6 CC            0920          CALL  TOCK
CC9B 06 12               0930          MVI   B,012H
CC9D CD A6 CC            0940          CALL  TOCK
CCA0 06 02               0950          MVI   B,002H
CCA2 CD A6 CC            0960          CALL  TOCK
CCA5 C9                  0970          RET
CCA6                     0975 * INCREMENT EACH DIGIT
CCA6 7E                  0980 TOCK     MOV   A,M
CCA7 3C                  0990          INR   A
CCA8 27                  1000          DAA
CCA9 B8                  1010          CMP   B
CCAA 77                  1020          MOV   M,A
```

```
CCAB C2 B2 CC            1030          JNZ    NCAR
CCAE 36 00               1040          MVI    M,0
CCB0 23                  1050          INX    H
CCB1 C9                  1060          RET
CCB2 F1                  1070 NCAR     POP    PSW
CCB3 C9                  1080          RET
CCB4 CD 1C CC            1090 TEST     CALL   COUNT
CCB7 21 00 FE            1100          LXI    H,0FE00H
CCBA 2C                  1110 DELAY    INR    L
CCBB C2 BA CC            1120          JNZ    DELAY
CCBE 24                  1130          INR    H
CCBF C2 BA CC            1140          JNZ    DELAY
CCC2 C3 B4 CC            1150          JMP    TEST
CCC5                     9000 *
```

SYMBOL TABLE

```
COUNT CC1C    DELAY CCBA    DISP  CC42    FACE  CC16    NCAR  CCB2    PBIAS 008C
START CC00    TEST  CCB4    TICK  CC87    TOCK  CCA6    WRT2  CC70
```

```
$D CC00 CCC4
CC00 21 38 00 36 C3 21 1C CC 22 39 00 3E FB 32 00 00
CC10 3E 08 D3 FD FB C9 10 01 00 14 00 01 E5 F5 21 00
CC20 00 39 31 00 CF E5 C5 D5 21 16 CC CD 87 CC 21 16
CC30 CC 7E B6 CC 42 CC 3E 08 D3 FD D1 C1 E1 F9 F1 E1
CC40 FB C9 11 3F D0 23 CD 70 CC 23 36 AE EB 1B CD 70
CC50 CC 36 BA EB 1B CD 70 CC 36 BA EB 1B CD 70 CC EB
CC60 46 EB 36 AD 2B 36 CD 2B AF B8 36 C1 C8 36 D0 C9
CC70 7E E6 0F F6 B0 EB 77 EB 1B 7E 1F 1F 1F 1F E6 0F
CC80 F6 B0 EB 77 2B 13 C9 06 12 CD A6 CC 06 10 CD A6
CC90 CC 06 60 CD A6 CC 06 60 CD A6 CC 06 12 CD A6 CC
CCA0 06 02 CD A6 CC C9 7E 3C 27 B8 77 C2 B2 CC 36 00
CCB0 23 C9 F1 C9 CD 1C CC 21 00 FE 2C C2 BA CC 24 C2
CCC0 BA CC C3 B4 CC

$
```

TROUBLE SHOOTING HINTS

THE CPU BOARD IS A SOPHISTICATED MICROPROCESSOR WITH MANY TIME SEQUENCED OPERATIONS. COMPREHENSIVE TROUBLE SHOOTING TECHNIQUES REQUIRE THE USE OF A HIGH SPEED OSCILLOSCOPE, AND INTIMATE KNOWLEDGE OF 8080A OPERATION. THE HINTS PROVIDED HERE WILL ALLOW THE USER TO REPAIR A BOARD FOR 90% OF MOST FAILURES, SINCE THEY ARE USUALLY ASSEMBLY ERRORS, SHORTS OR OBVIOUSLY FAILED PARTS.

IF THE CPU BOARD FAILS TO FUNCTION PROPERLY, MAKE THE FOLLOWING CHECKS:

1. CAREFULLY INSPECT FOR SOLDER SHORTS. A MINISCULE AMOUNT OF SOLDER ACROSS 2 PRINTED TRACES IS ALL THAT IS NEEDED FOR A SHORT.
2. CAREFULLY INSPECT FOR A CRACK IN A PC TRACE. THIS TYPE OF FAILURE HAS A LOWER PROBABILITY OF OCCURING.
3. CHECK THE POLARITY OF ALL DIODES AND ELECTROLYTIC CAPACITORS.
4. INSURE THAT ALL ICs ARE PROPERLY INSTALLED WITH RESPECT TO PIN ORIENTATION. (SEE THE ASSEMBLY DRAWING) THE MOST COMMON ASSEMBLY ERROR ENCOUNTERED IS WHEN THE IC PINS ARE BENT UNDER THE CHIP. CAREFULLY INSPECT FOR THIS TYPE OF MISTAKE.
5. IF AN EXTENDER BOARD IS BEING USED, AND YOU EXPERIENCE SEEMINGLY GHOST LIKE FAILURES, INSERT THE CPU BOARD DIRECTLY IN THE MOTHERBOARD. TRANSIENT NOISE CAN BE CAUSED BY EXTENDER BOARDS.

EXPERIMENTING WITH YOUR NEW COMPUTER

NOW THAT YOUR SHINY NEW COMPUTER IS ASSEMBLED AND CHECKED OUT, WHAT IS THE NEXT STEP? IF YOU HAVE NOT ALREADY DONE SO, YOU SHOULD READ THE INTEL 8080 MICROCOMPUTER SYSTEMS USER'S MANUAL AND BECOME FAMILIAR WITH THE INSTRUCTION SET AND EXACTLY WHAT GOES ON IN THE CPU CHIP FROM A PROGRAMMERS POINT OF VIEW. THE NEXT STEP WOULD BE TO TRY YOUR HAND AT SOME SIMPLE ASSEMBLY LANGUAGE PROGRAMS. LENGTHY PROGRAMS ARE USUALLY WRITTEN WITH THE AID OF AN ASSEMBLER PROGRAM WHICH ENORMOUSLY SIMPLIFIES THE TASK OF MAKING CHANGES IN THE PROGRAM, SUCH AS ESP-1 WHICH IS AVAILABLE FROM VECTOR GRAPHIC INC. AT A NOMINAL CHARGE.

SHORT PROGRAMS CAN BE CODED BY HAND USING AN 8080 PROGRAMMING CARD AND THEN ENTERED IN THE COMPUTER MEMORY USING THE VECTOR 1 MONITOR. ASSEMBLY LANGUAGE PROGRAMMING CONSISTS OF BUILDING A PROGRAM USING GENERAL PURPOSE SUBROUTINES AS BUILDING BLOCKS. MOST PROGRAMS HAVE ROUTINES THAT READ THE KEYBOARD, OUTPUT TO A PRINTER, CONVERT FROM HEX TO BINARY AND BACK, COMPARE ADDRESSES AND SO ON. AN EXPERIENCED PROGRAMMER WILL HAVE A COLLECTION OF THESE ROUTINES IN HIS "BAG OF TRICKS" THAT HE CAN INSERT IN A PROGRAM WHEN NEEDED. THE DIFFICULT PART IS TO BE ABLE TO QUICKLY SCAN THROUGH THE ROUTINE AND UNDERSTAND EXACTLY WHAT IT DOES, HOW DATA IS PASSED BACK AND FORTH, AND WHICH REGISTERS ARE USED TO SEE IF IT INTERFERES WITH THE USE OF REGISTERS IN THE CALLING ROUTINE. IF THERE IS A CONFLICT, THE REGISTER CONTENTS MUST BE PUSHED ON THE STACK BEFORE THE ROUTINE IS CALLED AND POPPED BACK AFTER A RETURN.

A USEFUL COLLECTION OF SUBROUTINES IS CONTAINED IN THE VECTOR 1 MONITOR, AND THEY CAN BE CALLED BY ANY PROGRAM YOU WISH TO WRITE. AN EXAMPLE OF A SHORT PROGRAM CALLED SRCH IS SHOWN IN FIGURE 1. THE PURPOSE OF SRCH IS TO LOOK FOR SPECIFIC INSTRUCTIONS SUCH AS INPUT OR OUTPUT COMMANDS IN A LARGE PROGRAM. THIS PROGRAM WAS ASSEMBLED USING ESP-1 TO RUN IN RAM ON THE PROM/RAM BOARD AND CALLS SUBROUTINES FROM THE MONITOR. THE PROGRAM IS TYPED IN USING LINE NUMBERS TO IDENTIFY LINES IN THE FILE. THE FIRST INSTRUCTION IN CALL AHEX, A SUBROUTINE IN THE MONITOR THAT INPUTS FOUR HEX DIGITS FROM THE KEYBOARD, ECHOES THEM TO THE PRINTER, CONVERTS THEM TO A 16 BIT BINARY ADDRESS IN REGISTERS H & L AND EXCHANGES H & L WITH D & E (REFER TO MONITOR LISTING). TWO SUCCESSIVE CALLS TO AHEX RESULT IN A STARTING ADDRESS IN H & L, AND AN ENDING ADDRESS IN D & E. THE NEXT INSTRUCTIONS SAVE H, SET UP REGISTERS TO CONVERT ONLY 2 CHARACTERS TO BINARY AND THEN CALL A PORTION OF AHEX TO INPUT A TWO DIGIT INSTRUCTION CODE FROM THE KEYBOARD. THIS CODE IS PUT IN REGISTER B, AND H IS RESTORED.

THE NEXT BLOCK OF INSTRUCTIONS IS REPEATED OVER AND OVER, SO A LABEL CONT IS GIVEN TO THIS POINT IN THE PROGRAM. MEMORY IS READ USING THE ADDRESS IN H & L AND COMPARED TO THE DESIRED OP CODE. IF THEY ARE NOT THE SAME, THE PROGRAM JUMPS TO SKP. IF THEY ARE THE SAME, PROGRAM EXECUTION PROCEEDS BY READING THE NEXT MEMORY LOCATION AND CALLING ERR WHICH PRINTS THE ADDRESS, OP CODE AND NEXT CODE IN THE PROPER FORMAT. BMP COMPARES THE CURRENT ADDRESS WITH THE FINISH ADDRESS IN D & E TO SEE IF IT IS TIME TO STOP, AND IF NOT, THE PROGRAM JUMPS BACK TO CONT TO CONTINUE THE SEARCH.

STARTING AT LINE 0200 ARE FOUR INSTRUCTIONS CALLED PSEUDO OP CODES THAT SERVE TO GIVE THE ASSEMBLER ADDITIONAL INFORMATION IT NEEDS, NAMELY WHERE THE SUBROUTINES ARE ACTUALLY LOCATED. THE PARTICULAR ASSEMBLER USED REQUIRES THAT THE ADDRESSES IN HEX BE PRECEDED BY A 0 AND FOLLOWED BY H TO DENOTE HEX. NO OBJECT CODE IS GENERATED BY THESE INSTRUCTIONS. THE CODE PRODUCED BY THE ASSEMBLER IS SHOWN ON THE LEFT OF THE LISTING FOLLOWING THE 4 DIGIT HEX MEMORY LOCATION. MANY OF THE INSTRUCTIONS GENERATE MULTIBYTE CODES, AND THESE ARE LOADED IN SUBSEQUENT MEMORY LOCATIONS.

THE ASSEMBLER PRINTS AN ALPHABETICAL TABLE OF ALL THE LABELS USED IN THE PROGRAM FOLLOWED BY THE CORRESPONDING ADDRESS, SO THAT THESE POINTS CAN BE REFERENCED IN SUBSEQUENT PROGRAMS. BELOW THE SYMBOL TABLE, THE PROGRAM WAS EXECUTED BY TYPING G CC00 FROM THE MONITOR. THE ADDRESS RANGE OF C000 TO CIFF (THE MONITOR PROGRAM) WAS ENTERED AND THEN D3, THE 8080 CODE FOR "OUT". THE PROGRAM RESPONDED BY PRINTING OUT ALL LOCATIONS WHERE THE OUTPUT INSTRUCTION OCCURRED IN THE MONITOR PROGRAM FOLLOWED BY THE PORT NUMBER. YOU CAN TRY THIS ON YOUR SYSTEM BY ENTERING THE OBJECT CODE IN THE PROPER MEMORY LOCATION USING THE "P" MONITOR COMMAND.

FIGURE 1 EXPERIMENTING WITH YOUR NEW COMPUTER

```
A CC00
  MEM  LOC
CC00 CD 57 C0          0010 SRCH   CALL   AHEX        START
CC03 CD 57 C0          0020        CALL   AHEX        FINISH(S=H,F=D)
CC06 E5                0030        PUSH   H           SAVE H
CC07 2E 00             0040        MVI    L,0
CC09 0E 02             0050        MVI    C,2         COUNT OF 2
CC0B CD 5C C0          0060        CALL   AHE1        READ 2 DIGITS
CC0E EB                0070        XCHG               H=CODE,D=F
CC0F 45                0080        MOV    B,L         PUT CODE IN B
CC10 E1                0090        POP    H           RESTORE H
CC11 7E                0100 CONT   MOV    A,M         READ MEMORY
CC12 B8                0110        CMP    B           COMPARE TO CODE
CC13 C2 1C CC          0120        JNZ    SKP         SKIP IF NO COMP
CC16 23                0130        INX    H           INCR ADDRESS
CC17 7E                0140        MOV    A,M         READ NEXT BYTE
CC18 2B                0150        DCX    H           DECR ADDRESS
CC19 CD 68 C1          0160        CALL   ERR         PRINT CODES
CC1C CD F5 C1          0170 SKP    CALL   BMP         CHECK IF DONE
CC1F C2 11 CC          0180        JNZ    CONT        BACK FOR MORE
CC22 C9                0190        RET
CC23                   0200 BMP    EQU    0C1F5H
CC23                   0210 ERR    EQU    0C168H
CC23                   0220 AHE1   EQU    0C05CH
CC23                   0230 AHEX   EQU    0C057H

SYMBOL TABLE

AHE1  C05C   AHEX  C057   BMP   C1F5   CONT  CC11   ERR   C168   SKP   CC1C
SRCH  CC00

G C000

*G CC00 C000 C1FF D3
C008 D3 10
C00C D3 10
C07E D3 01
C0C8 D3 6F
C0CE D3 6E
*G CC00 C000 C1FF DB
C076 DB 00
C08B DB 00
C092 DB 01
C0C0 DB 6E
C0EE DB C0
C10F DB 6E
C116 DB 6F
*
```

GENERAL TROUBLE SHOOTING GUIDE

BECAUSE OF THE COMPLEXITY OF THE ENTIRE COMPUTER SYSTEM, BOTH THE HARDWARE AND SOFTWARE, IT IS ESSENTIAL TO ISOLATE ANY PROBLEM TO AN INDIVIDUAL BOARD OR PROGRAM. FORTUNATELY, ALL OF THE COMPUTER LOGIC IS ON EASILY REMOVABLE BOARDS. IT IS EXTREMELY VALUABLE TO HAVE ACCESS TO A TESTED COMPUTER SO THAT THE BOARDS CAN BE INDIVIDUALLY TESTED. ALTHOUGH THERE IS THE POSSIBILITY OF INTERACTION BETWEEN BOARDS DUE TO MARGINAL TIMING, OR DEFECTIVE COMPONENTS, THIS IS NOT THE USUAL CASE, AND IT IS BEST TO ASSUME THAT IF A BOARD WORKS IN COMPUTER A IT WILL ALSO WORK IN COMPUTER B.

THE MINIMUM SYSTEM CONSISTS OF THREE BOARDS, THE CPU BOARD, THE PROM/RAM BOARD, AND EITHER A VIDEO OR SERIAL I/O BOARD. MAKE SURE THAT THE MONITOR PROGRAM HAS BEEN PROPERLY PATCHED FOR THE PARTICULAR I/O CONFIGURATION OF YOUR SYSTEM. THERE IS TOTAL CONFUSION IN THE INDUSTRY CONCERNING PORT ASSIGNMENTS, LOGIC CONVENTIONS, AND STRAPPING OPTIONS. SEVERAL TYPES OF PROGRAMMABLE USARTS ARE USED WHICH REQUIRE INITIALIZATION.

IF YOU HAVE CAREFULLY FOLLOWED THE ASSEMBLY INSTRUCTION FOR EACH OF THE BOARDS AND THE REGULATORS CHECK OUT, INSTALL ALL CHIPS. LET'S ASSUME YOU ARE USING A VIDEO DISPLAY. AS SOON AS YOU TURN THE COMPUTER ON, YOU SHOULD SEE A DISPLAY OF RANDOM MEMORY GARBAGE ON THE TV SCREEN. THIS WILL BE INDEPENDENT OF ANY FUNCTIONING OF THE COMPUTER OTHER THAN THE CLOCK OSCILLATOR. IF YOU DO NOT GET A PROPER DISPLAY, THE VIDEO INTERFACE MUST BE DEBUGGED FIRST. FEEL THE CHIPS ON THE BOARD. ANY THAT ARE HOT TO THE TOUCH MAY BE IN BACKWARDS (PROBABLY DESTROYED OF TTL) OR MAY HAVE THEIR OUTPUTS SHORTED. THERE IS MORE THAN A FACTOR OF TEN DIFFERENCE IN THE POWER DISSIPATION OF TTL CHIPS, BUT THEY SHOULD NOT BE UNCOMFORTABLY HOT TO THE TOUCH.

REMOVE THE BOARD AND INSPECT IT CAREFULLY. ABOUT HALF OF THE PROBLEMS CAN BE FOUND SIMPLY BY VISUAL INSPECTION. LOOK WITH A MAGNIFYING GLASS OR INSPECTION SCOPE AT EACH PIN ON THE BOTTOM FOR UNSOLDERED PINS, MISSING PINS THAT MAY BE BENT UNDER OR BROKEN OFF, *SOLDER BRIDGES BETWEEN PINS OR TO ADJACENT* TRACES, AND ETCH BRIDGES BETWEEN TRACES (VERY HARD TO SEE). A CAREFUL EXAMINATION WILL TAKE 15 MINUTES, BUT MAY SAVE YOU A LOT OF GRIEF, AND YOU MAY DISCOVER PROBLEMS LIKE UNSOLDERED PINS THAT MAY REVEAL THEMSELVES ONLY LATER AS INTERMITTENT PROBLEMS. EXAMINE THE TOP OF THE BOARD TO BE SURE THE PROPER CHIPS ARE INSTALLED IN THE RIGHT PLACES. SIGHT ALONG THE EDGE OF THE CHIPS TO FIND BENT UNDER PINS. CHIPS ARE SOMETIMES INSERTED WITH A WHOLE ROW OF PINS THAT MISS THE SOCKET HOLES.

IF THE VISUAL INSPECTION FAILS TO GET THE VIDEO DISPLAY WORKING, A COMPONENT MAY BE BAD (USUALLY AN IC). TRY EXCHANGING IDENTICAL COMPONENTS TO SEE IF THE SYMPTOMS CHANGE. AT THIS POINT IT IS WISE TO GO BACK AND CAREFULLY REREAD THE MANUAL TO BE SURE YOU UNDERSTAND THE WAY THE BOARD WORKS AND THAT YOU HAVE SELECTED THE PROPER JUMPER OPTIONS. AFTER THIS, YOU WILL PROBABLY WANT TO TAKE THE UNIT TO A DEALER IF YOU ARE NOT FAMILIAR WITH DIGITAL TROUBLE SHOOTING PROCEDURES, OR GO THROUGH THE CIRCUIT BLOCK BY BLOCK WITH A SCOPE OR LOGIC PROBE IF YOU ARE EXPERIENCED.

AFTER THE VIDEO DISPLAY OR SERIAL I/O IS WORKING, THE RESET SWITCH SHOULD CAUSE A "*" PROMPT TO BE WRITTEN. IF THIS DOES NOT WORK, FOLLOW THE SAME PROCEDURE ON THE CPU AND PROM/RAM BOARDS. THE CPU BOARD CONSISTS MOSTLY OF 8097 BUS DRIVERS WHICH CAN BE EXCHANGED ONE BY ONE. THE VECTORED INTERRUPT AND REAL TIME CLOCK COMPONENTS, IC TBD. TBD ARE NOT NECESSARY IN THE BOARD AT THIS TIME AND SHOULD BE REMOVED. USING A SCOPE, EXAMINE THE OUTPUT PINS OF ALL CHIPS. LOW LOGIC LEVELS ARE NORMALLY LESS THAN 0.2 VOLTS AND HIGH GREATER THAN 3.0 VOLTS. A LEVEL OF 0.4 VOLTS MAY INDICATE SHORTS BETWEEN OUTPUTS WHERE ONE IS TRYING TO PULL HIGH AND THE OTHER LOW. A LEVEL OF 1.2 VOLTS INDICATES AN OPEN CIRCUITED INPUT. NMOS CHIPS HAVE SIMILAR LOGIC LEVELS, WHILE PMOS CHIPS CAN PULL TTL INPUTS TO -0.6V WHERE THE INPUT CLAMP DIODE LIMITS THE VOLTAGE. DO NOT BE SURPRISED AT HOW STRANGE SOME OF THE WAVEFORMS ON THE BUS LOOK, SUCH AS THE DI LINES. THERE ARE PERIODS OF TIME DURING WHICH THE BUS IS NOT BEING ACTIVELY DRIVEN, AND THE VOLTAGE MAY DRIFT DUE TO RECEIVER INPUT CURRENT. ABNORMAL OPERATION IS INDICATED PRINCIPALLY BY ABNORMAL LOGIC LEVELS MAINTAINED CONSTANT FOR AT LEAST ONE CLOCK PERIOD (500 MICROSECONDS).

ONCE YOUR BASIC SYSTEM IS WORKING, CHECK OUT OF MEMORY BOARDS AND OTHER INTERFACES IS RELATIVELY STRAIGHTFORWARD USING THE MEMORY TEST PROGRAM IN THE MONITOR, OR SIMPLY DIAGNOSTIC ROUTINES YOU CAN PROGRAM IN MEMORY ON THE PROM/RAM BOARD. AFTER YOUR SYSTEM IS UP AND RUNNING, IT SHOULD BE QUITE RELIABLE. SINCE MOST MICROCOMPUTER SYSTEMS ARE MEMORY INTENSIVE, THE MEMORY IS THE MOST LIKELY SOURCE OF COMPONENT FAILURE. A SYSTEM WITH 32 K OF STATIC MEMORY MAY CONTAIN 75% OF ITS COMPONENTS ON THE MEMORY BOARDS. IF A PROBLEM IS EXPERIENCED RUNNING A PROGRAM, FIRST SUSPECT THE MEMORY AND USE THE MONITOR TEST PROGRAM. WE HAVE YET TO EXPERIENCE A PROBLEM WITH OUR 8K MEMORY BOARDS THAT WAS NOT REVEALED BY THE TEST PROGRAM. IF YOU DO MUCH REARRANGING OF YOUR SYSTEM, IT IS A GOOD PRACTICE TO TEST MEMORY FOR A FEW SECONDS WHEN YOU FIRST TURN ON THE COMPUTER TO MAKE SURE THE BOARDS ARE ADDRESSED PROPERLY OR THAT THEY ARE IN THE COMPUTER. THIS MAY SAVE SOME HEAD SCRATCHING WHEN THE PROGRAM YOU HAVE JUST LOADED FAILS TO RESPOND TO YOUR EAGER KEYBOARD TOUCH. IF YOU SUSPECT TEMPERATURE SENSITIVE CHIPS, REMOVE THE COVER OF THE COMPUTER TO INTERRUPT AIR FLOW BETWEEN BOARDS. WE DO NOT RECOMMEND OBSTRUCTING THE AIR FLOW THROUGH THE COMPUTER BY PLACING A SHEET OF PAPER OVER THE LEFT SIDE. A FULL COMPUTER MAY DISSIPATE OVER 300 WATTS AND REACH UNACCEPTABLE TEMPERATURES IF NO AIRFLOW IS PERMITTED.

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ERRATA - CPU BOARD REV. 2

AN ERROR ON THE CPU BOARD REV. 2 RESULTS IN THE RESTART ADDRESSES GOING TO THE S-100 BUS IN IMPROPER ORDER.

A LOW ON PIN	11	OF THE S-100 WILL GIVE A RESTART	7.
"	10	"	4
"	9	"	2
"	8	"	6
"	7	"	1
"	6	"	5
"	5	"	3
"	4	"	0

IF THE USER NEEDS THE PROPER ORDER OF RESTART ADDRESSES:

1. CUT THE TRACE FROM PIN 10 OF THE 8214 TO PIN 9 OF THE 8212.
2. CUT THE TRACE FROM PIN 8 OF THE 8214 TO PIN 18 OF THE 8212.
3. INSTALL A JUMPER FROM PIN 10 OF THE 8214 TO PIN 18 OF THE 8212.
4. INSTALL A JUMPER FROM PIN 8 OF THE 8214 TO PIN 9 OF THE 8212.

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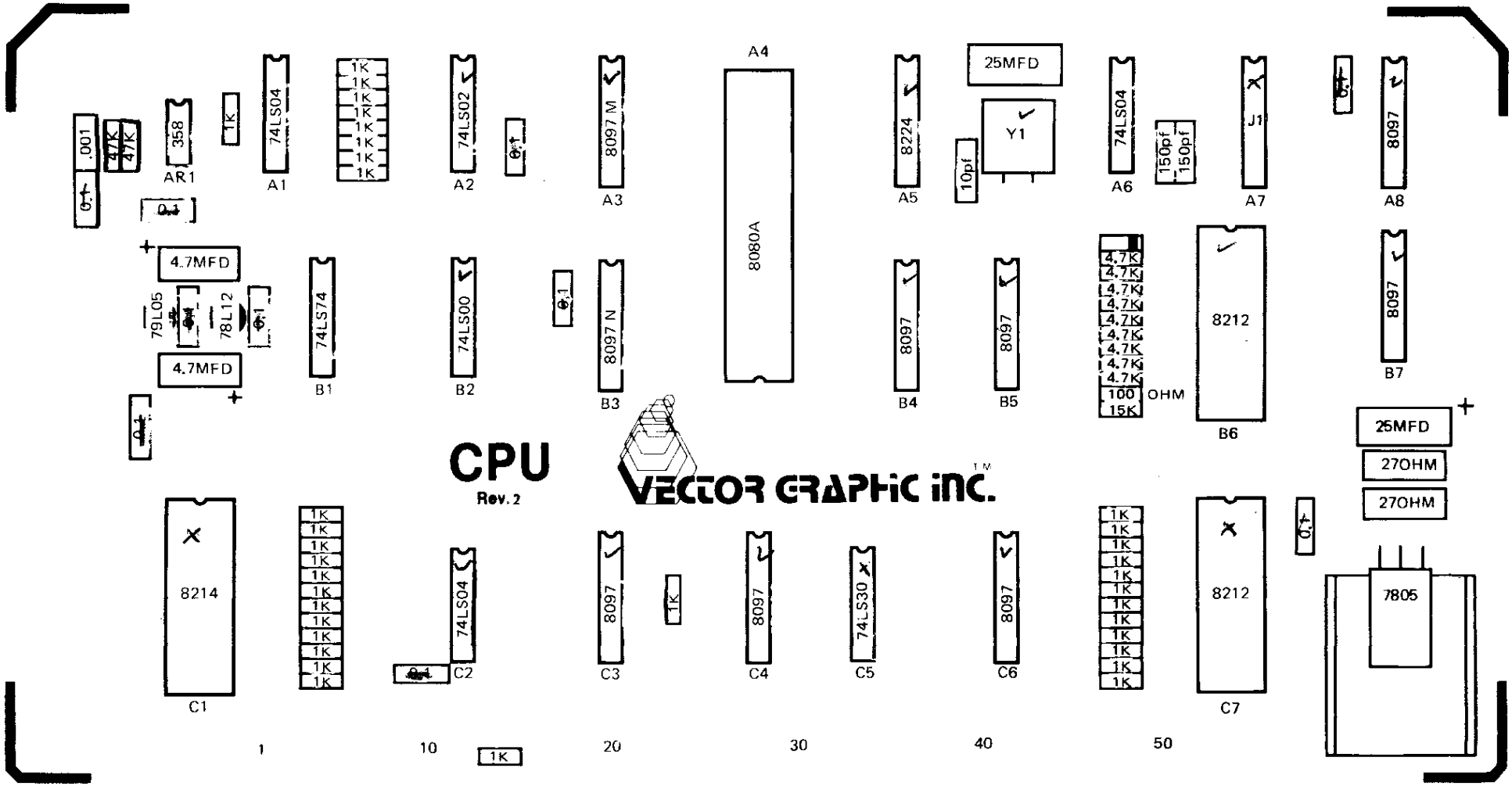
CPU
Rev. 2
VECTOR GRAPHIC INC.
.001
47K
47K
358
AR1
1K
74LS04
A1
1K
1K
1K
1K
1K
1K
74LS02
A2
8097 M
A3
8080A
A4
8224
A5
25MFD
Y1
10pf
74LS04
A6
150pf
150pf
J1
A7
8097
A8
4.7MFD
79L05
78L12
4.7MFD
74LS74
B1
74LS00
B2
8097 N
B3
8097
B4
8097
B5
4.7K
4.7K
4.7K
4.7K
4.7K
4.7K
4.7K
4.7K
4.7K
100
15K
OHM
8212
B6
8097
B7
25MFD
27OHM
27OHM
7805
8214
C1
1K
1K
1K
1K
1K
1K
1K
1K
1K
1K
74LS04
C2
8097
C3
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8097
C4
74LS30
C5
8097
C6
1K
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8212
C7
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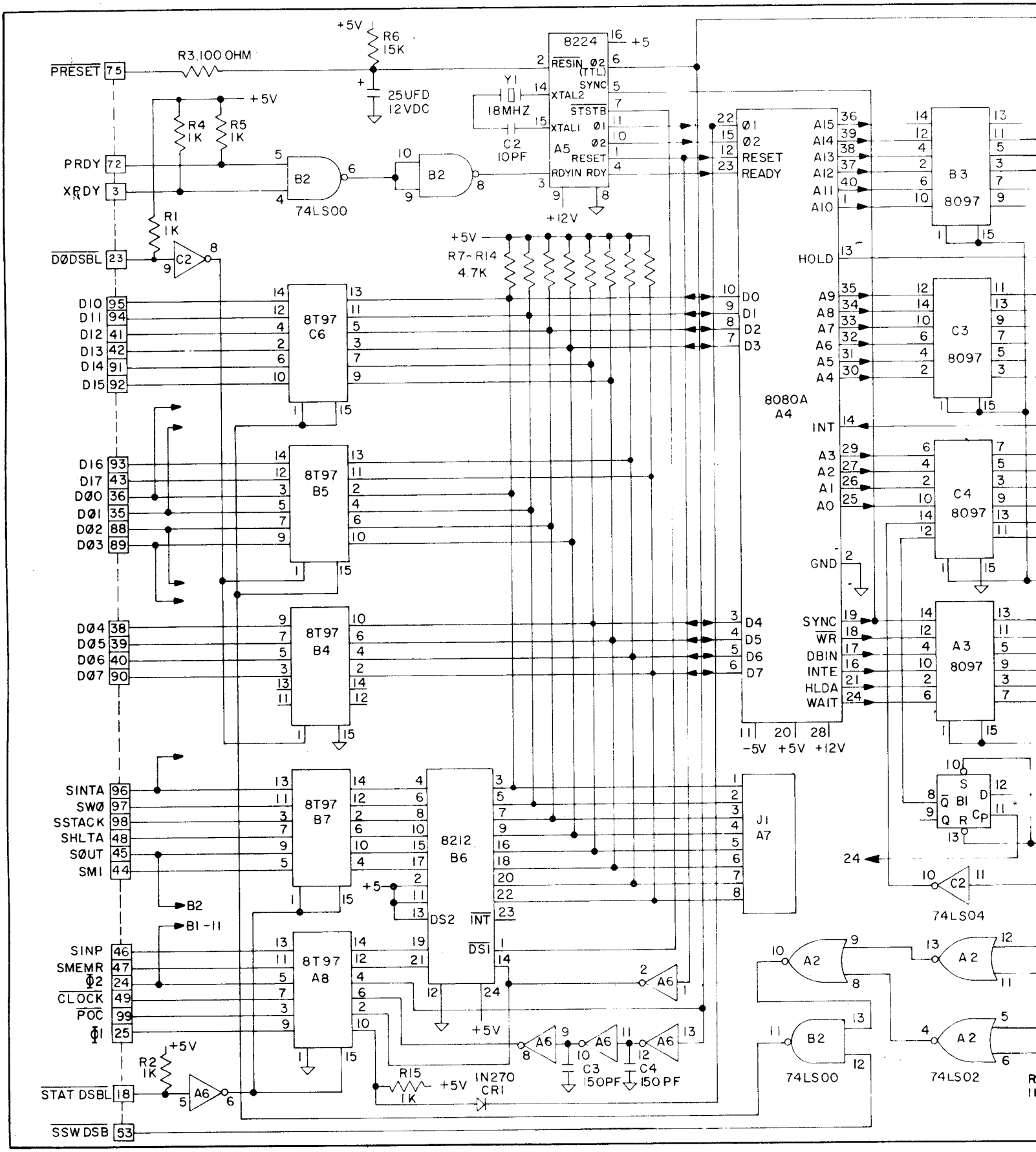
1K
20
30
40
50


PRESET 75
R3, 100 OHM
+5V
R6 15K
25UFD 12VDC
8224
RESIN
(TTL)
SYNC
XTAL2
STSTB
XTAL1
A5
RESET
RDYIN
Y1 18MHZ
C2 10PF
+12V
PRDY 72
XRDY 3
R4 1K
R5 1K
B2
74LS00
R1 1K
DØDSBL 23
C2
R7-R14 4.7K
DI0 95
DI1 94
DI2 41
DI3 42
DI4 91
DI5 92
8T97 C6
DI6 93
DI7 43
DØ0 36
DØ1 35
DØ2 88
DØ3 89
8T97 B5
DØ4 38
DØ5 39
DØ6 40
DØ7 90
8T97 B4
SINTA 96
SWØ 97
SSTACK 98
SHLTA 48
SØUT 45
SMI 44
8T97 B7
8212 B6
DS2
INT
DSI
J1 A7
B2
B1-11
SINP 46
SMEMR 47
Φ2 24
CLOCK 49
POC 99
Φ1 25
8T97 A8
R2 1K
STAT DSBL 18
SSW DSB 53
R15 1K
IN270 CR1
C3 150PF
C4 150PF
A6
A2
74LS02
74LS04
8080A A4
HOLD
INT
GND
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WAIT
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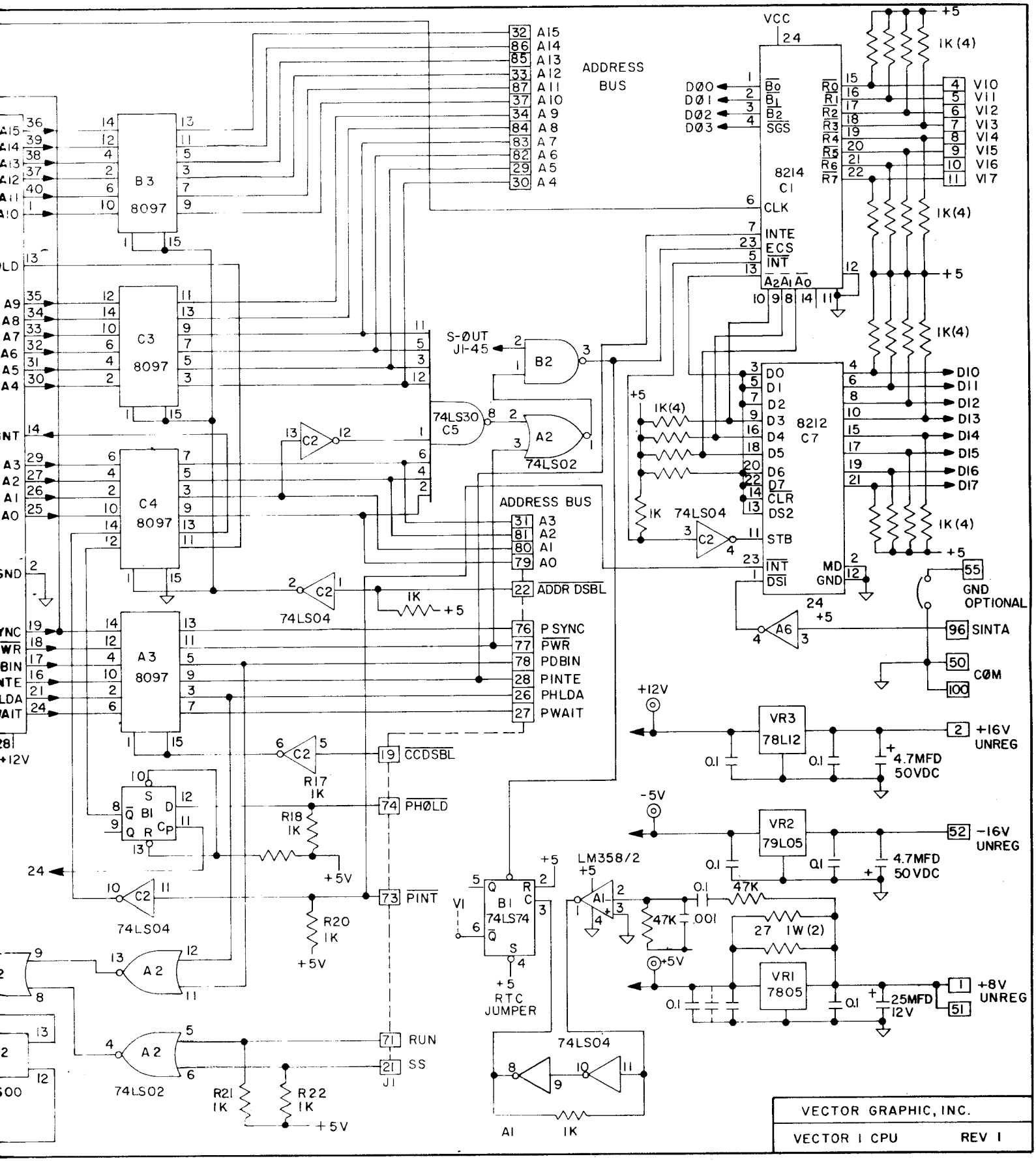

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VECTOR I CPU	REV I